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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/082,816	02/25/2002	Andrew Cofler	00GR35154360	1555

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EXAMINER	
TSAI, HENRY	

ART UNIT	PAPER NUMBER
2183	

DATE MAILED: 11/10/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/082,816	COFLER ET AL.	
	Examiner	Art Unit	
	Henry W.H. Tsai	2183	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on 5/31/02.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) 25-49 is/are pending in the application.

4a) Of the above claim(s) _ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) 25-27,30,36-40 and 50 is/are rejected.

7)☒ Claim(s) 28,29,31-35 and 41-49 is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☒ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on 5/31/02 is/are: a)☐ accepted or b)☒ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Note this supplemental Office Action is issued due to the preliminary amendment mailed 2/25/02 was not considered. The previous Office Action mailed 9/21/04 has been vacated.

Drawings

1. The drawings are objected to as failing to comply with 37 CFR 1.84(p)(5) because they do not include the following reference sign(s) mentioned in the description: "MC3" (at page 23, line 24). Corrected drawing sheets in compliance with 37 CFR 1.121(d) are required in reply to the Office action to avoid abandonment of the application. Any amended replacement drawing sheet should include all of the figures appearing on the immediate prior version of the sheet, even if only one figure is being amended. The replacement sheet(s) should be labeled "Replacement Sheet" in the page header (as per 37 CFR 1.84(c)) so as not to obstruct any portion of the drawing figures. If the changes are not accepted by the examiner, the applicant will be notified and informed of any required corrective action in the

next Office action. The objection to the drawings will not be held in abeyance.

Specification

2. The disclosure is objected to because of the following informalities: at page 21, line 15, "RGC" should read -GRC-.

Appropriate correction is required.

Claim Rejections - 35 USC § 102

3. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless -

> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

4. Claims 25-27, 36-40, and 50 are rejected under 35 U.S.C. 102(e) as being anticipated by Emma et al. (U.S. Patent No. 5,353,421) (hereafter referred to as Emma et al.'421).

Referring to claim 25, Emma et al.'421 discloses, as claimed, a method of handling branching instructions using a

processor (see Fig. 10, and col. 14, lines 14-15) comprising a program memory (10, see Fig. 10, and Col. 7, lines 3-5) storing program instructions, and a processor core comprising a plurality of processing units (certainly existing in the Emma et al.'421's system, such as integer unit, floating point unit, and addressing unit) and a central unit (certainly existing in the Emma et al.'421's system, such as the CPU) connected thereto, the central unit issuing instructions to the processing units based upon the program instructions, the method comprising: clocking the processor core with a clock signal (since a clock is certainly used to synchronize the processing in the Emma et al.'421's system); receiving a branching instruction (based on the branch address see Fig. 12) in the course of a current cycle; and processing the received branching instruction in the current cycle (with broadest reasonable interpretation, the Emma et al.'421's system will process a branching instruction immediately without wait when the instruction is received, see pipeline stages in Fig. 1).

Referring to claim 36, Emma et al.'421 discloses, as claimed, a method of handling branching instructions using a processor (see Fig. 10, and col. 14, lines 14-15) comprising a program memory (10, see Fig. 10, and Col. 7, lines 3-5) storing program instructions, and a processor core comprising a

plurality of processing units (certainly existing in the Emma et al.'421's system, such as integer unit, floating point unit, and addressing unit), and a central unit (certainly existing in the Emma et al.'421's system, such as the CPU) connected thereto, the central unit issuing instructions to the processing units based upon the program instructions, the method comprising: receiving at the central core a branching instruction (based on the branch address see Fig. 12) during a current clock cycle and processing the received branching instruction during the current clock cycle (with broadest reasonable interpretation, the Emma et al.'421's system will process a branching instruction immediately without wait when the instruction is received, see pipeline stages in Fig. 1).

Referring to claim 38, Emma et al.'421 discloses, as claimed, a processor (see Fig. 10, and col. 14, lines 14-15) comprising: a program memory (10, see Fig. 10, and Col. 7, lines 3-5) for storing program instruction; and a processor core being clocked by a clock signal (since a clock is certainly used to synchronize the processing in the Emma et al.'421's system) and comprising a plurality of processing units (certainly existing in the Emma et al.'421's system, such as integer unit, floating point unit, and addressing unit) and a central unit (certainly existing in the Emma et al.'421's system, such as the CPU)

connected thereto, said central unit for issuing instructions to said processing units based upon corresponding program instructions; said central unit comprising a branching module (instruction buffer 11, see Fig. 10) for receiving a branching instruction (based on the branch address see Fig. 12) during a current clock cycle, and processing this branching instruction during the current clock cycle (with broadest reasonable interpretation, the Emma et al.'421's system will process a branching instruction immediately without wait when the instruction is received, see pipeline stages in Fig. 1).

As to claims 26, 37, and 39, Emma et al.'421 also discloses: the processing units comprise a first processing unit including at least one address-pointing register (inside BHT 82, see Fig. 9); wherein a branching instruction uses the content of the at least one address-pointing register (inside BHT 82, see Fig. 9); and further comprising checking validity (validity bit V, see Fig. 9 and 11, see also Col. 13, lines 54-56) of the content of the at least one address-pointing register (inside BHT 82, see Fig. 9) at the start of the current cycle so that the branching instruction is actually received by the central unit and processed if the content is declared valid (when the validity bit V is valid, see Fig. 9 and 11, see also Col. 13, lines 54-56), and, in an opposite case (when the

validity bit V is not valid, see Fig. 9 and 11, see also Col. 13, lines 54-56), the branching instruction is kept on hold (since the target of the branch found in BHT will not be fetched when the validity bit V is valid, see Col. 13, lines 54-56) for processing until the content is declared valid.

As to claims 27, and 40, Emma et al.'421 also discloses: recopying the content of the at least one address-pointing register into at least- one corresponding duplicated address-pointing register (the register, not explicitly shown, inside the select logic 105 or select gate 106 for storing the inputs); and wherein the checking (note the validity of the bit V shown in Fig. 9 is checked by the select logic 105 see Fig. 11) is of the at least one corresponding duplicated address-pointing register.

As to claim 50, Emma et al.'421 also discloses: having a decoupled architecture (since the instruction cycle of the Emma et al.'421's system comprises different pipelined stages involving Instruction fetch or prefetch and Operand fetch and using different units in parallel see Fig. 1).

Claim Rejections - 35 USC § 103

5. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

6. Claim 30 is rejected under 35 U.S.C. 103(a) as being unpatentable over Emma et al.'421 in view of European Patent Application No. EP 1 050 805 (hereafter referred to as EP'805) or Applicant Admitted Prior Art mentioned in Specification page 4, last paragraph to page 5, lines 1-18 (hereafter referred to as AAPA).

Emma et al.'421 discloses the claimed invention except for a second processing unit including a guard-indication register, wherein in the presence of a guarded branching instruction, a check on the validity of the guard indication assigned to the branching instruction and contained in the guard-indication register is carried out at the start of the current cycle; and wherein the guarded branching instruction is actually received

by the central unit and processed, if the value of the corresponding guard indication is declared valid, and, in the opposite case, this guarded branching instruction is kept on hold for processing until the value of the corresponding guard indication is declared valid (in claim 30).

EP'805 discloses a system comprising a second processing unit (19, see Fig. 1) contains a guard-indication register (100, see Fig. 1), wherein in the presence of a guarded branching instruction, a check on the validity of the value of the guard indication assigned to said branching instruction (see Col. 5, lines 54-55, regarding the guard selecting from G0-G15 selected for each instruction (certainly including branch instruction)) and contained in the guard-indication register (100, see Fig. 1) is carried out at the start of said current cycle, and in that said guarded branching instruction is actually received by the central unit (12, see Fig. 1) and processed, if the value of the corresponding guard indication (see Col. 2, lines 44-49 or Col. 5, lines 54-55, regarding the guard selecting from G0-G15 selected for each instruction (certainly including branch instruction)) is declared valid (see Col. 5, lines 56-58, regarding the value true or false attributed to guards from G0-G15 is however dependent upon the guard values held at any particular time in a guard register file), and, in the opposite

case, this guarded branching instruction is kept on hold for processing until the value of the corresponding guard indication is declared valid. Besides, as Applicant Admitted Prior Art mentioned in Specification page 4, last paragraph to page 5, lines 1-18, the use of guarded instruction in a processor is already known in to a person skilled in the art.

It would have been obvious to one having ordinary skill in the art at the time the invention was made to modify Emma et al.'421's system to comprise a second processing unit including a guard-indication register, wherein in the presence of a guarded branching instruction, a check on the validity of the guard indication assigned to the branching instruction and contained in the guard-indication register is carried out at the start of the current cycle; and wherein the guarded branching instruction is actually received by the central unit and processed, if the value of the corresponding guard indication is declared valid, and, in the opposite case, this guarded branching instruction is kept on hold for processing until the value of the corresponding guard indication is declared valid, as taught by EP'805 (or AAPA), in order to facilitate efficiently controlling the branch instructions by reduce the latency due to data dependency and pipeline stall problems (such

as using predicates, see Col. 1, lines 27-28) for the Emma et al.'421's device.

Allowable Subject Matter

7. Claims 28, 29, 31-35, and 41-49 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

Conclusion

8. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure. Kahle et al.'002 discloses a recovery from hang condition in a microprocessor. The completion unit is adapted to produce a completion valid signal responsive to the issue unit completing an instruction. The hang detect unit is configured to receive the completion valid signal from the ISU and adapted to determine the interval since the most recent assertion of the completion valid signal. Matsuo et al.'587 discloses a data processor calculating branch target address of a branch instruction in parallel with decoding of the instruction. A branch target address calculation unit 1 which is connected to the instruction fetch unit 111 and the

program counter (DPC) 29, adds a value of a branch displacement field transferred from the instruction fetch unit 111 and the instruction address transferred from the program counter (DPC) 29.

Contact Information

9. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Dr. Henry Tsai whose telephone number is (571) 272-4176. The examiner can normally be reached on Monday-Thursday from 8:00 AM to 5:00 PM. If attempts to reach the examiner by telephone are unsuccessful, the examiner supervisor, Eddie Chan, can be reached on (571) 272-4162. Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to **the TC central telephone number, 571-272-2100.**

10. In order to reduce pendency and avoid potential delays, Group 2100 is encouraging FAXing of responses to Office actions directly into **the Group at fax number: 703-872-9306.** This practice may be used for filing papers not requiring a fee. It

may also be used for filing papers which require a fee by applicants who authorize charges to a PTO deposit account. Please identify the examiner and art unit at the top of your cover sheet. Papers submitted via FAX into Group 2100 will be promptly forward to the examiner.

HENRY W. H. TSAI
PRIMARY EXAMINER

November 4, 2004